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EXAMINER	
LI, AIMEE J	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 12/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/545,040	COL ET AL.
	Examiner	Art Unit
	Aimee J. Li	2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2005 and 27 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31 and 33-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31 and 33-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-31, 33-34, and new claims 35-44 have been considered. New claims 35-44 have been added as per Applicant's request. Claims 1, 10, 21, 22, and 30 have been amended as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as filed 18 March 2005; Amendment as filed 17 June 2005; and 27 September 2005.

Allowable Subject Matter

3. Claims 21-22, 30-33, and 35-43 are allowed.

4. The following is an examiner's statement of reasons for allowance: Independent claims 21 and 30 each contain similar limitations to, taking claim 21 as exemplary, "first and second virtual address comparators", "first and second physical address comparators", and "stalling the pipeline subsequent to said forwarding logic forwarding said storehit data from said store buffer if said physical match signal indicates a match between said physical load address and said second physical store address although said virtual match signal previously indicated no match between said virtual load address and said second virtual store address, until correct data specified by said physical load address is provided to replace said previously forwarded second storehit data". The prior art searched taught virtual address comparators or physical address comparators, but not many taught both in a single system. The prior searched did teach using both virtual address and physical address comparators using one or the other comparator but not using the physical address comparator to double check whether the virtual address comparator

was correct and stalling the pipeline depending on the result of the second comparison. Claim 35 is similar to claims 21 and 30, however, instead of stalling the pipeline, the results from the second store instruction is forwarded when the first comparator result is found to be incorrect. This is also not taught in the prior art. The prior art searched that came closest to this type of functionality was found in branch prediction mechanisms. However, there was nothing found in any of the searched prior art that would motivate one of ordinary skill in the art at the time the invention was made to incorporate these types of branch prediction mechanisms in speculative result forwarding mechanisms.

5. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-20 and 26-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abramson et al., U.S. Patent Number 5,606,670 (herein referred to as Abramson) in view of Hughes, U.S. Patent Number 6,662,280 (herein referred to as Hughes).

8. Referring to claim 1, Abramson has taught an apparatus within a pipelined microprocessor for forwarding store instruction results to a pipeline stage for execution of a load

instruction (Abramson Abstract; column 1, lines 18-30; column 2, lines 43 to column 3, line3; column 4, line 56 to column 5, line 19; column 5, line 49 to column 6t, line 13; column 7, lines 59-56; column 8, lines 9-49; column 9, lines 1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7), the apparatus comprising:

a. A result forwarding cache (RFC), for storing a plurality of store instruction results destined for a data cache of the microprocessor (Abramson Abstract; column 1, lines 18-30; column 2, lines 43 to column 3, line3; column 4, line 56 to column 5, line 19; column 5, line 49 to column 6t, line 13; column 7, lines 59-56; column 8, lines 9-49; column 9, lines 1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7);

b. Comparison logic, for comparing a load address of the load instruction with a plurality of store addresses associated with said plurality of store instruction results to generate an address match signal (Abramson Abstract; column 1, lines 18-30; column 2, lines 43 to column 3, line3; column 4, line 56 to column 5, line 19; column 5, line 49 to column 6t, line 13; column 7, lines 59-56; column 8, lines 9-49; column 9, lines 1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7); and

c. Control logic, configured to receive said match signal and selectively forward one of said plurality of store instruction results from said RFC to the pipeline stage in response to said match signal, thereby avoiding stalling the load instruction until said one of said plurality of store instruction results is updated into said data cache (Abramson Abstract; column 1, lines 18-30; column 2, lines 43 to column 3,

line3; column 4, line 56 to column 5, line 19; column 5, line 49 to column 6t, line 13; column 7, lines 59-56; column 8, lines 9-49; column 9, lines 1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7).

9. Abramson has not taught storing at least one non-store instruction result destined for a user-visible register of the microprocessor. However, Abramson has taught storing and forwarding store operation results (Abramson Abstract; column 1, lines 18-30; column 2, lines 43 to column 3, line3; column 4, line 56 to column 5, line 19; column 5, line 49 to column 6t, line 13; column 7, lines 59-56; column 8, lines 9-49; column 9, lines 1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7). Hughes has taught storing results is not only for results of store instructions but also other arithmetic instructions that require results to be written to memory (Hughes column 1, lines 28-42). A person of ordinary skill in the art at the time the invention was made would have recognized that storing store results for all operations that require a store in the instruction, not only store instructions, allows the results of all operations to access the results of the instructions, thereby improving data consistency and efficiency, since the system does not need to continue repeating the same instructions to find the same results. The results can just be retrieved from its storage location. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate storing results for all store operations, not only store instructions, to improve data consistency and efficiency of the system.

10. Referring to claim 2, Abramson in view of Hughes has taught wherein said plurality of store instruction results comprise data to be stored from the microprocessor into a memory

attached thereto (Abramson Abstract; column 1, lines 18-30; column 2, lines 43 to column 3, line3; column 4, line 56 to column 5, line 19; column 5, line 49 to column 6t, line 13; column 7, lines 59-56; column 8, lines 9-49; column 9, lines 1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7).

11. Referring to claim 3, Abramson in view of Hughes has taught wherein said load address specifies a location of data to be loaded into the microprocessor from a memory attached thereto (Abramson Abstract; column 1, lines 18-30; column 2, lines 43 to column 3, line3; column 4, line 56 to column 5, line 19; column 5, line 49 to column 6t, line 13; column 7, lines 59-56; column 8, lines 9-49; column 9, lines 1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7).

12. Referring to claim 4, Abramson in view of Hughes has taught wherein said RFC comprises a plurality of storage elements for storing a predetermined number of instruction results (Abramson Abstract; column 1, lines 18-30; column 2, lines 43 to column 3, line3; column 4, line 56 to column 5, line 19; column 5, line 49 to column 6t, line 13; column 7, lines 59-56; column 8, lines 9-49; column 9, lines 1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7).

13. Referring to claim 5, Abramson in view of Hughes has taught wherein said instruction results are received by said RFC from an execution unit of the microprocessor (Abramson Abstract; column 1, lines 18-30; column 2, lines 43 to column 3, line3; column 4, line 56 to column 5, line 19; column 5, line 49 to column 6t, line 13; column 7, lines 59-56; column 8, lines 9-49; column 9, lines 1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7).

14. Referring to claim 6, Abramson in view of Hughes has taught wherein said plurality of storage elements store said predetermined number of instruction results in a first-in-first-out manner (Abramson Abstract; column 1, lines 18-30; column 2, lines 43 to column 3, line3; column 4, line 56 to column 5, line 19; column 5, line 49 to column 6t, line 13; column 7, lines 59-56; column 8, lines 9-49; column 9, lines 1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7).

15. Referring to claim 7, Abramson in view of Hughes has taught wherein said predetermined number of instruction results is five (Abramson Abstract; column 1, lines 18-30; column 2, lines 43 to column 3, line3; column 4, line 56 to column 5, line 19; column 5, line 49 to column 6t, line 13; column 7, lines 59-56; column 8, lines 9-49; column 9, lines 1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7).

16. Referring to claim 8, Abramson in view of Hughes has taught wherein said load address and said plurality of store addresses comprise virtual addresses (Abramson Abstract; column 1, lines 18-30; column 2, lines 43 to column 3, line3; column 4, line 56 to column 5, line 19; column 5, line 49 to column 6t, line 13; column 7, lines 59-56; column 8, lines 9-49; column 9, lines 1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7).

17. Referring to claim 9, Abramson in view of Hughes has taught wherein said virtual addresses comprise x86 linear addresses (Abramson Abstract; column 1, lines 18-30; column 2, lines 43 to column 3, line3; column 4, line 56 to column 5, line 19; column 5, line 49 to column

6t, line 13; column 7, lines 59-56; column 8, lines 9-49; column 9, lines 1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7).

18. Referring to claim 10, Abramson has taught an apparatus for forwarding storehit data within stages of a pipelined microprocessor, the apparatus comprising:

a. A result forwarding cache (RFC), to store and forward a first plurality of store instruction results destined for a data cache of the microprocessor (Abramson Abstract; column 1, lines 18-30; column 2, lines 43 to column 3, line3; column 4, line 56 to column 5, line 19; column 5, line 49 to column 6t, line 13; column 7, lines 59-56; column 8, lines 9-49; column 9, lines 1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7);

b. A data unit, configured to forward a second plurality of store instruction results (Abramson Abstract; column 1, lines 18-30; column 2, lines 43 to column 3, line3; column 4, line 56 to column 5, line 19; column 5, line 49 to column 6t, line 13; column 7, lines 59-56; column 8, lines 9-49; column 9, lines 1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7); and

c. Selection logic, coupled to said RFC and said data unit, for selectively providing one of said first and second plurality of store instruction results to a stage of the microprocessor pipeline executing a load instruction (Abramson Abstract; column 1, lines 18-30; column 2, lines 43 to column 3, line3; column 4, line 56 to column 5, line 19; column 5, line 49 to column 6t, line 13; column 7, lines 59-56; column

8, lines 9-49; column 9, lines 1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7).

19. Abramson has not taught configured to forward at least one non-store instruction result. However, Abramson has taught storing and forwarding store operation results (Abramson Abstract; column 1, lines 18-30; column 2, lines 43 to column 3, line3; column 4, line 56 to column 5, line 19; column 5, line 49 to column 6t, line 13; column 7, lines 59-56; column 8, lines 9-49; column 9, lines 1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7). Hughes has taught storing results is not only for results of store instructions but also other arithmetic instructions that require results to be written to memory (Hughes column 1, lines 28-42). A person of ordinary skill in the art at the time the invention was made would have recognized that storing store results for all operations that require a store in the instruction, not only store instructions, allows the results of all operations to access the results of the instructions, thereby improving data consistency and efficiency, since the system does not need to continue repeating the same instructions to find the same results. The results can just be retrieved from its storage location. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate storing results for all store operations, not only store instructions, to improve data consistency and efficiency of the system.

20. Referring to claim 11, Abramson in view of Hughes has taught wherein said load instruction comprises a load address for specifying an address of data to be loaded into the microprocessor (Abramson Abstract; column 1, lines 18-30; column 2, lines 43 to column 3, line3; column 4, line 56 to column 5, line 19; column 5, line 49 to column 6t, line 13; column 7,

lines 59-56; column 8, lines 9-49; column 9, lines 1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7), wherein said selection logic is configured to forward one of said first and second plurality of store instruction results only if said load address matches one or more of a first and second plurality of store addresses corresponding to said first and second plurality of store instruction results (Abramson Abstract; column 1, lines 18-30; column 2, lines 43 to column 3, line3; column 4, line 56 to column 5, line 19; column 5, line 49 to column 6t, line 13; column 7, lines 59-56; column 8, lines 9-49; column 9, lines 1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7).

21. Referring to claim 12, Abramson in view of Hughes has taught wherein selection logic forwards said first plurality of store instruction results forwarded by said RFC at a higher priority than said second plurality of store instructions results forwarded by said data unit if said load address matches both one or more of said first plurality of store addresses and one or more of said second plurality of store addresses (Abramson Abstract; column 1, lines 18-30; column 2, lines 43 to column 3, line3; column 4, line 56 to column 5, line 19; column 5, line 49 to column 6t, line 13; column 7, lines 59-56; column 8, lines 9-49; column 9, lines 1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7).

22. Referring to claim 13, Abramson in view of Hughes has taught comparison logic, coupled to said selection logic, for comparing said load address with said first and second plurality of store addresses to determine whether said load address matches one or more of said first and second plurality of store addresses (Abramson Abstract; column 1, lines 18-30; column 2, lines 43 to column 3, line3; column 4, line 56 to column 5, line 19; column 5, line 49 to

column 6t, line 13; column 7, lines 59-56; column 8, lines 9-49; column 9, lines 1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7).

23. Referring to claim 14, Abramson in view of Hughes has taught wherein said data unit is configured to forward said second plurality of store instruction results from a plurality of store buffers of the microprocessor (Abramson Abstract; column 1, lines 18-30; column 2, lines 43 to column 3, line3; column 4, line 56 to column 5, line 19; column 5, line 49 to column 6t, line 13; column 7, lines 59-56; column 8, lines 9-49; column 9, lines 1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7).

24. Referring to claim 15, Abramson in view of Hughes has taught wherein said plurality of store buffers is configured to store said second plurality of store instruction results while said second plurality of store instruction results are written to a memory coupled to the microprocessor (Abramson Abstract; column 1, lines 18-30; column 2, lines 43 to column 3, line3; column 4, line 56 to column 5, line 19; column 5, line 49 to column 6t, line 13; column 7, lines 59-56; column 8, lines 9-49; column 9, lines 1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7).

25. Referring to claim 16, Abramson in view of Hughes has taught wherein said data unit is configured to forward a newest one of said second plurality of store instruction results if said load address matches more than one of said second plurality of store addresses (Abramson Abstract; column 1, lines 18-30; column 2, lines 43 to column 3, line3; column 4, line 56 to column 5, line 19; column 5, line 49 to column 6t, line 13; column 7, lines 59-56; column 8, lines 9-49; column 9, lines 1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7).

26. Referring to claim 17, Abramson in view of Hughes has taught wherein said RFC is configured to forward a newest one of said first plurality of store instruction results if said load address matches more than one of said first plurality of store addresses (Abramson Abstract; column 1, lines 18-30; column 2, lines 43 to column 3, line3; column 4, line 56 to column 5, line 19; column 5, line 49 to column 6t, line 13; column 7, lines 59-56; column 8, lines 9-49; column 9, lines 1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7).

27. Referring to claim 18, Abramson has taught an apparatus for detecting storehit conditions in a pipelined microprocessor in a hierarchical manner, the apparatus comprising:

a. First comparison logic, for comparing a load instruction load address in a first stage of the pipeline with a first plurality of store addresses of first store instruction data in a plurality of stages of the pipeline subsequent to said first pipeline stage (Abramson Abstract; column 1, lines 18-30; column 2, lines 43 to column 3, line3; column 4, line 56 to column 5, line 19; column 5, line 49 to column 6t, line 13; column 7, lines 59-56; column 8, lines 9-49; column 9, lines 1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7);

b. Second comparison logic, for comparing said load address with a second plurality of store addresses of second store instruction data in a plurality of store buffers of the microprocessor (Abramson Abstract; column 1, lines 18-30; column 2, lines 43 to column 3, line3; column 4, line 56 to column 5, line 19; column 5, line 49 to column 6t, line 13; column 7, lines 59-56; column 8, lines 9-49; column 9, lines

1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7); and

c. Control logic, coupled to said first and second comparison logic, configured to determine which of said first and second store instruction data is newest based on said first and second comparison logic comparing, and to forward said newest store instruction data to said first pipeline stage in response thereto (Abramson Abstract; column 1, lines 18-30; column 2, lines 43 to column 3, line3; column 4, line 56 to column 5, line 19; column 5, line 49 to column 6t, line 13; column 7, lines 59-56; column 8, lines 9-49; column 9, lines 1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7).

28. Abramson has not taught wherein said plurality of stages of the pipeline subsequent to said first pipeline stage comprise non-store buffers. Hughes has taught wherein said plurality of stages of the pipeline subsequent to said first pipeline stage comprise non-store buffers (Hughes column 12, lines 4-23; column 13, lines 26-35; and Figure 2). In regards to Hughes, the reorder buffer and data cache are connected to the circuit and accept data from the system at stages after the first stage comparison (Hughes column 12, lines 4-23; column 13, lines 26-35; column 14, lines 40-60; and Figure 2). A person of ordinary skill in the art at the time the invention was made would have recognized that the reorder buffer of Hughes ensure instruction dependency order is maintained, thereby ensuring data consistency and correctness, and the data cache allows data to be accessed at any time, thereby ensuring correct execution in the system. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was

made to incorporate Hughes in the device of Abramson to ensure data consistency and correct execution of the instructions.

29. Referring to claim 19, Abramson has taught wherein said first comparison logic is configured to compare virtual addresses (Abramson Abstract; column 1, lines 18-30; column 2, lines 43 to column 3, line3; column 4, line 56 to column 5, line 19; column 5, line 49 to column 6t, line 13; column 7, lines 59-56; column 8, lines 9-49; column 9, lines 1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7).

30. Referring to claim 20, Abramson has taught wherein said second comparison logic is configured to compare physical addresses (Abramson Abstract; column 1, lines 18-30; column 2, lines 43 to column 3, line3; column 4, line 56 to column 5, line 19; column 5, line 49 to column 6t, line 13; column 7, lines 59-56; column 8, lines 9-49; column 9, lines 1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7)

31. Referring to claim 26, Abramson has taught a method for forwarding storehit data in a microprocessor pipeline, the method comprising:

a. Storing at least one store instruction result into a result forwarding cache of the microprocessor (Abramson Abstract; column 1, lines 18-30; column 2, lines 43 to column 3, line3; column 4, line 56 to column 5, line 19; column 5, line 49 to column 6t, line 13; column 7, lines 59-56; column 8, lines 9-49; column 9, lines 1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7);

b. Detecting a storehit condition, wherein a load instruction in a stage of the pipeline specifies data generated by a previous store instruction, wherein said data is still

present in the pipeline (Abramson Abstract; column 1, lines 18-30; column 2, lines 43 to column 3, line3; column 4, line 56 to column 5, line 19; column 5, line 49 to column 6t, line 13; column 7, lines 59-56; column 8, lines 9-49; column 9, lines 1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7);

c. Determining whether said data is present in said result forwarding cache; selectively forwarding said data from said result forwarding cache to said stage if said data is in said result forwarding cache (Abramson Abstract; column 1, lines 18-30; column 2, lines 43 to column 3, line3; column 4, line 56 to column 5, line 19; column 5, line 49 to column 6t, line 13; column 7, lines 59-56; column 8, lines 9-49; column 9, lines 1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7); and

d. Selectively forwarding said data from a data unit of the microprocessor to said stage if said data is not in said result forwarding cache (Abramson Abstract; column 1, lines 18-30; column 2, lines 43 to column 3, line3; column 4, line 56 to column 5, line 19; column 5, line 49 to column 6t, line 13; column 7, lines 59-56; column 8, lines 9-49; column 9, lines 1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7).

32. Abramson has not taught storing at least one non-store instruction result into a result forwarding cache of the microprocessor. However, Abramson has taught storing and forwarding store operation results (Abramson Abstract; column 1, lines 18-30; column 2, lines 43 to column 3, line3; column 4, line 56 to column 5, line 19; column 5, line 49 to column 6t, line 13; column

7, lines 59-56; column 8, lines 9-49; column 9, lines 1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7). Hughes has taught storing results is not only for results of store instructions but also other arithmetic instructions that require results to be written to memory (Hughes column 1, lines 28-42). A person of ordinary skill in the art at the time the invention was made would have recognized that storing store results for all operations that require a store in the instruction, not only store instructions, allows the results of all operations to access the results of the instructions, thereby improving data consistency and efficiency, since the system does not need to continue repeating the same instructions to find the same results. The results can just be retrieved from its storage location. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate storing results for all store operations, not only store instructions, to improve data consistency and efficiency of the system.

33. Referring to claim 27, Abramson in view of Hughes has taught storing results data of each store instruction executed by an execution unit of the microprocessor in said result forwarding cache (Abramson Abstract; column 1, lines 18-30; column 2, lines 43 to column 3, line3; column 4, line 56 to column 5, line 19; column 5, line 49 to column 6t, line 13; column 7, lines 59-56; column 8, lines 9-49; column 9, lines 1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7).

34. Referring to claim 28, Abramson in view of Hughes has taught wherein said detecting said storehit condition comprises:

a. Comparing an address of said data specified by said load instruction with a plurality of store instruction result data addresses stored in the pipeline below said

stage (Abramson Abstract; column 1, lines 18-30; column 2, lines 43 to column 3, line3; column 4, line 56 to column 5, line 19; column 5, line 49 to column 6t, line 13; column 7, lines 59-56; column 8, lines 9-49; column 9, lines 1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7); and

b. Determining said address matches one or more of said plurality of data addresses (Abramson Abstract; column 1, lines 18-30; column 2, lines 43 to column 3, line3; column 4, line 56 to column 5, line 19; column 5, line 49 to column 6t, line 13; column 7, lines 59-56; column 8, lines 9-49; column 9, lines 1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7).

35. Referring to claim 29, Abramson in view of Hughes has taught wherein said determining whether said data is present in said result forwarding cache comprises:

a. Comparing an address of said data specified by said load instruction with a plurality of store instruction result data addresses stored in a predetermined number of stages of the pipeline below said stage (Abramson Abstract; column 1, lines 18-30; column 2, lines 43 to column 3, line3; column 4, line 56 to column 5, line 19; column 5, line 49 to column 6t, line 13; column 7, lines 59-56; column 8, lines 9-49; column 9, lines 1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7);

b. Wherein said predetermined number equals a number of result entries in said result forwarding cache (Abramson Abstract; column 1, lines 18-30; column 2,

lines 43 to column 3, line3; column 4, line 56 to column 5, line 19; column 5, line 49 to column 6t, line 13; column 7, lines 59-56; column 8, lines 9-49; column 9, lines 1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7).

36. Claims 23-25 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abramson et al., U.S. Patent Number 5,606,670 (herein referred to as Abramson) in view of Young, U.S. Patent Number 5,933,844 (herein referred to as Young).

37. Referring to claim 23, Abramson has taught a pipelined microprocessor for speculatively forwarding storehit data from a first pipeline stage to a second pipeline stage, wherein the storehit data is specified by a load address in the second stage, comprising:

a. Forwarding logic, for forwarding the storehit data from the first stage to the second stage prior to said address region logic generating said match signal (Abramson Abstract; column 1, lines 18-30; column 2, lines 43 to column 3, line3; column 4, line 56 to column 5, line 19; column 5, line 49 to column 6t, line 13; column 7, lines 59-56; column 8, lines 9-49; column 9, lines 1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7);

b. Control logic, configured to receive said match signal and to assert a stall signal, subsequent to said forwarding logic forwarding the storehit data, to stall the pipeline, and to subsequently obtain using the load address non-cached correct data from a device external to the microprocessor, for provision to the second stage (Abramson Abstract; column 1, lines 18-30; column 2, lines 43 to column 3,

line3; column 4, line 56 to column 5, line 19; column 5, line 49 to column 6t, line 13; column 7, lines 59-56; column 8, lines 9-49; column 9, lines 1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7).

38. Abramson has not explicitly taught address region logic, configured to receive the load address and generate a match signal to indicate whether the load address is within one of a plurality of non-cacheable address regions of the microprocessor address space stored therein. However, Abramson has taught that a type of result forwarding for store operations based upon the virtual addresses (Abramson Abstract; column 1, lines 18-30; column 2, lines 43 to column 3, line3; column 4, line 56 to column 5, line 19; column 5, line 49 to column 6t, line 13; column 7, lines 59-56; column 8, lines 9-49; column 9, lines 1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7), which means that the system speeds up, since it is no longer necessary to translate the addresses into physical addresses, which takes at least 1 cycle, to check if there is an address match. Abramson also teaches that there must be checks to ensure the validity of the data being forwarded (Abramson Abstract; column 1, lines 18-30; column 2, lines 43 to column 3, line3; column 4, line 56 to column 5, line 19; column 5, line 49 to column 6t, line 13; column 7, lines 59-56; column 8, lines 9-49; column 9, lines 1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7). However, Young has taught that the physical address of data may indicate that the address region is in a non-cacheable region (Young column 1, lines 46-63) to avoid data consistency problems. Therefore, it would have been obvious to a person of ordinary

skill in the art at the time the invention was made to incorporate the non-cacheable region of Young in the device of Abramson to avoid data consistency problems.

39. Referring to claim 24, Abramson in view of Young has taught

a. A bus interface unit, for receiving data from a bus coupled to the microprocessor, said bus further coupled to a system memory and a plurality of peripheral devices (Abramson Figure 1); and

b. At least one response buffer, operatively coupled to the second stage, for receiving load data specified by the load address from said bus interface unit, and for providing said load data to the second stage to replace the storehit data if the load address is within one of said plurality of non-cacheable address regions (Abramson Abstract; column 1, lines 18-30; column 2, lines 43 to column 3, line3; column 4, line 56 to column 5, line 19; column 5, line 49 to column 6t, line 13; column 7, lines 59-56; column 8, lines 9-49; column 9, lines 1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7).

40. Referring to claim 25, Abramson in view of Young has taught wherein said plurality of non-cacheable regions stored in said address region logic are software-programmable (Young column 1, lines 46-63).

41. Referring to claim 34, Abramson has taught a method for speculatively forwarding storehit data in a microprocessor pipeline, the method comprising:

a. Detecting a storehit condition by comparing a load address with a plurality of store addresses (Abramson Abstract; column 1, lines 18-30; column 2, lines 43 to

column 3, line3; column 4, line 56 to column 5, line 19; column 5, line 49 to column 6t, line 13; column 7, lines 59-56; column 8, lines 9-49; column 9, lines 1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7);

b. Forwarding storehit data in response to said detecting said storehit condition (Abramson Abstract; column 1, lines 18-30; column 2, lines 43 to column 3, line3; column 4, line 56 to column 5, line 19; column 5, line 49 to column 6t, line 13; column 7, lines 59-56; column 8, lines 9-49; column 9, lines 1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7); and

c. Stalling the pipeline (Abramson Abstract; column 1, lines 18-30; column 2, lines 43 to column 3, line3; column 4, line 56 to column 5, line 19; column 5, line 49 to column 6t, line 13; column 7, lines 59-56; column 8, lines 9-49; column 9, lines 1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7).

42. Abramson has not explicitly taught determining said load address is within a non-cacheable address region subsequent to said speculatively forwarding. However, Abramson has taught that a type of result forwarding for store operations based upon the virtual addresses (Abramson Abstract; column 1, lines 18-30; column 2, lines 43 to column 3, line3; column 4, line 56 to column 5, line 19; column 5, line 49 to column 6t, line 13; column 7, lines 59-56; column 8, lines 9-49; column 9, lines 1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7), which means that the system speeds up,

since it is no longer necessary to translate the addresses into physical addresses, which takes at least 1 cycle, to check if there is an address match. Abramson also teaches that there must be checks to ensure the validity of the data being forwarded (Abramson Abstract; column 1, lines 18-30; column 2, lines 43 to column 3, line3; column 4, line 56 to column 5, line 19; column 5, line 49 to column 6t, line 13; column 7, lines 59-56; column 8, lines 9-49; column 9, lines 1-43; column 9, line 66 to column 10, line 3; column 11, lines 12-17; Figure 2; Figure 5; Figure 6; and Figure 7). However, Young has taught that the physical address of data may indicate that the address region is in a non-cacheable region (Young column 1, lines 46-63) to avoid data consistency problems. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the non-cacheable region of Young in the device of Abramson to avoid data consistency problems.

Response to Arguments

43. The Examiner would like to note that the primary reference is the same Abramson patent used in previous rejections was used again. However, after reconsidering the claims and Abramson, it was felt that the arguments with regard to the combination of Abramson with the other cited references in the previous Office Action did not meet all limitation in the claims and that Abramson actually contained more teachings than originally thought by the Examiner.

44. Applicant's arguments, see Amendment, filed 27 September 2005, with respect to the rejection(s)of claim(s) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of the above.

Conclusion

45. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

a. Tran et al., U.S. Patent Number 6,065,103, has taught a speculative store buffer that forwards results to a load instruction.

46. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

47. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

48. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
7 December 2005

Eddie C

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